REMARKS

Claims 1-49 are currently pending in the application. Claims 1-49 were rejected. Claims 1, 14-16, 21, 27, 28, 31, and 49 have been amended.

The Examiner objected to claims 14 and 21. The proposed amendment has been made and the objection is believed addressed thereby.

The Examiner rejected claims 23-26 and 45-48 under 35 U.S.C. 112, first paragraph as failing to comply with the enablement requirement. The rejection is respectfully traversed.

Claims 23-26 and 45-48 relate to various simulatable representations of the circuit and system of claims 1 and 28, respectively. As is well known in the art of semiconductor circuit design, and as pointed out by the Examiner, there are a wide variety of tools which facilitate the layout and design of such circuits. The use of these tools results in digital representations of the circuit designs, the operation of which may then be simulated so that the designers can further refine their designs. The choice of tools is often driven by the particular design style, the preferences of the designer, or both, and is so straightforward as to not even be worth mentioning from an enablement perspective. However, given that specific and well known tools (e.g., VHDL and Verilog) and simulatable representations (e.g., SPICE netlist) are actually called out in the present specification, and the fact that even those having a relatively low level of skill in the art understand how to use such tools to implement the functionality described, there is more than ample information provided in the present application to enable one of ordinary skill in the art to design and simulate the circuits and systems claimed. In view of the foregoing, the rejection is believed overcome.

The Examiner objected to claims 15, 16, 27, 31, 49 under 35 U.S.C. 112, second paragraph, for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. These claims have been amended and the objections are believed addressed thereby.

The Examiner rejected claims 1-14, 20, 22, 27-32, 34, 35, 37-42, 44, and 49 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,488,729 (Vegesna). The Examiner also rejected claims 15-19, 33, 36, 43, and 45-48 under 35 U.S.C. 103(a) as being unpatentable over Vegesna in view of a variety of other references. Claims 1, 27, 28, and 49 have been amended to more clearly described the invention and the rejections are believed overcome thereby.

More specifically, claim 1 has been amended to recite "issuance of the data units in the respective pipelines being staggered in time," and claim 28 has been amended to recite "the N-way issue resource being operable to issue the units of data in N parallel pipelines staggered in time." These amendments are supported in the present specification, for example, at paragraph [0022], and are clearly distinguishable from the system described in Vegesna which repeatedly stresses that a key aspect of its approach is that the instructions issued to its parallel pipelines are issued *simultaneously*. See, for example, column 1, lines 16-22; column 2, lines 56-61 and 64-67; column 3, lines 11-13; column 14, lines 59-61; column 23, lines 8-11; column 29, lines 34-37; etc.

It is clear that the simultaneous issuance of instructions in Vesegna's approach is not optional, but a fundamental aspect of his invention. Vegesna makes it clear that "[i]f insufficient resources exist to execute two core unit instructions simultaneously (i.e. they both require the same resource), only the first of the paired instructions will issue." See column 3, lines 1-3. Vesegna repeatedly stresses that this capability is not present in previous architectures. See, for example, column 3, lines 40-50, and the description of the shortcomings of "prior approaches" beginning at column 6, line 10, and referring to Figs. 1-17. Vesegna also stresses the importance of this feature in describing the benefits of his invention. See column 4, lines 18-22 and 35-40.

Vesegna represents an important computer architecture advance, but requires sophisticated algorithms to achieve the performance described. By contrast, specific embodiments of the invention offer a more straightforward approach which enables designers to

achieve the performance of multiple parallel issue without actually having to introduce the complex algorithms taught by Vesegna.

In view of the fact that Vesegna's architecture requires the simultaneous issuance of instructions in its pipelines, the rejection of claims 1 and 28 is believed overcome. In addition, the rejection of claim 2-27 and 29-49 is believed overcome for at least the reasons discussed.

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (510) 663-1100.

Respectfully submitted,
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